IN THE CLAIMS:

Claims 1-3, and 5-25 have been amended. All of the pending claims 1 through 25 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Currently Amended) A method for testing a plurality of semiconductor components, comprising:

forming a plurality of dice on a semiconductor wafer, ~~said~~ the plurality of dice each including at least one die contact; and

forming at least one wafer-level redistribution circuit on each of ~~said~~ the plurality of dice for interconnection with others of ~~said~~ the plurality of dice, ~~said~~ the at least one wafer-level redistribution circuit including a redistribution ~~circuit~~ circuit, and a bus conductor traversing each of ~~said~~ the plurality of dice for electrically coupling with at least another one of ~~said~~ the plurality of dice and at least one conductor for coupling ~~said~~ the redistribution circuit to ~~said~~ the bus conductor.

2. (Currently Amended) The method, as recited in claim 1, further comprising forming an outer passivation layer on an exposed face of ~~said~~ the semiconductor wafer covering ~~said~~ the redistribution circuit and ~~said~~ the bus conductor.

3. (Currently Amended) The method, as recited in claim 2, further comprising probing each of ~~said~~ the plurality of dice to determine functional and nonfunctional dice.

4. (Original) The method, as recited in claim 3, further comprising storing location information on nonfunctional dice.

5. (Currently Amended) The method, as recited in claim 4, further comprising isolating at least one die contact on each of ~~said~~ the nonfunctional dice.

6. (Currently Amended) The method, as recited in claim 5, wherein ~~said~~ isolating includes removing a portion of ~~said~~ the outer passivation layer over ~~said~~ the at least one of ~~said~~ the redistribution circuit and ~~said~~ the bus ~~connector~~ conductor to form an open circuit between ~~said~~ the at least one die contact and ~~said~~ the bus conductor on ~~said~~ the nonfunctional dice.

7. (Currently Amended) The method, as recited in claim 5, wherein ~~said~~ isolating includes ablating of at least a portion of ~~said~~ the at least one wafer-level redistribution circuit and ~~said~~ the outer passivation layer.

8. (Currently Amended) The method, as recited in claim 5, wherein ~~said~~ isolating includes etching of at least a portion of ~~said~~ the at least one wafer-level redistribution circuit and ~~said~~ the outer passivation layer.

9. (Currently Amended) A method for manufacturing wafer-level testable dice, comprising:

forming a plurality of dice on a semiconductor wafer, ~~said~~ the plurality of dice each including at least one die contact; and

forming at least one wafer-level redistribution circuit on each of ~~said~~ the plurality of dice for interconnection with others of ~~said~~ the plurality of dice, ~~said~~ the at least one wafer-level redistribution circuit including a redistribution circuit, and a bus conductor traversing each of ~~said~~ the plurality of dice for electrically coupling with at least another one of ~~said~~ the plurality of dice and at least one other bus conductor for coupling ~~said~~ the redistribution circuit to ~~said~~ the bus conductor.

10. (Currently Amended) The method, as recited in claim 9, further comprising isolating at least one of ~~said~~ the at least one die contact on nonfunctional dice of ~~said~~ the plurality of dice on ~~said~~ the semiconductor wafer.

11. (Currently Amended) The method, as recited in claim 9, further comprising probing each of ~~said~~ the plurality of dice to determine functional and nonfunctional dice of ~~said~~ the plurality of dice.

12. (Currently Amended) A method for fabricating a wafer-level testable semiconductor component, comprising:

forming a plurality of dice on a semiconductor wafer, ~~said~~ the plurality of dice each including at least one die contact;

forming at least one wafer-level redistribution circuit on each of ~~said~~ the plurality of dice for interconnection with others of ~~said~~ the plurality of dice, ~~said~~ the at least one wafer-level redistribution circuit including a redistribution circuit, and a bus conductor traversing each of ~~said~~ the plurality of dice for electrically coupling with at least another one of ~~said~~ the plurality of dice and at least one other bus conductor for coupling ~~said~~ the redistribution circuit to ~~said~~ the bus conductor;

isolating ~~said~~ the at least one die contact on each nonfunctional die of ~~said~~ the plurality of dice;

testing functional dice of ~~said~~ the plurality of dice while integral with ~~said~~ the semiconductor wafer; and

singulating one of ~~said~~ the functional dice of ~~said~~ the plurality of dice from ~~said~~ the semiconductor component.

13. (Currently Amended) The method, as recited in claim 12, wherein ~~said~~ isolating further comprises probing each of ~~said~~ the plurality of dice to determine ~~said~~ the functional dice and ~~said~~ the nonfunctional dice of ~~said~~ the plurality of dice.

14. (Currently Amended) The method, as recited in claim 12, further comprising burning-in ~~said~~ the semiconductor component while ~~said~~ the semiconductor component is integral with ~~said~~ the semiconductor wafer.

15. (Currently Amended) A method for retrofitting an existing wafer layout for wafer-level testing, comprising:

on a semiconductor wafer including a plurality of dice with each die including at least one die contact, forming at least one wafer-level redistribution circuit on each of ~~said~~ the plurality of dice for interconnection with others of ~~said~~ the plurality of dice, ~~said~~ the at least one wafer-level redistribution circuit including a redistribution circuit for coupling ~~said~~ the at least one die contact to a respective bumped contact, a bus conductor traversing at least a portion of each of ~~said~~ the plurality of dice for electrically coupling with at least another one of ~~said~~ the plurality of dice, ~~said~~ the at least one other bus conductor for coupling ~~said~~ the redistribution circuit to ~~said~~ the bus conductor; and

isolating at least one die contact on each nonfunctional die of ~~said~~ the plurality of dice.

16. (Currently Amended) The method, as recited in claim 15, wherein ~~said~~ forming further comprises forming an outer passivation layer over ~~said~~ the redistribution circuit and ~~said~~ the bus conductor.

17. (Currently Amended) The method, as recited in claim 15, wherein ~~said~~ isolating further comprises probing each of ~~said~~ the plurality of dice to determine functional dice and ~~said~~ the nonfunctional dice of ~~said~~ the plurality of dice.

18. (Currently Amended) The method, as recited in claim 16, wherein ~~said~~ isolating includes removing a portion of ~~said~~ the outer passivation layer over ~~said~~ the at least one ~~of said~~ wafer-level redistribution circuit and forming an open circuit between ~~said~~ the at least one die contact and ~~said~~ the bus conductor on ~~said~~ the nonfunctional dice.

19. (Currently Amended) The method, as recited in claim 18, wherein ~~said~~ isolating includes ablating of at least a portion of ~~said~~ the at least one wafer-level redistribution circuit and ~~said~~ the outer passivation layer.

20. (Currently Amended) The method, as recited in claim 18, wherein ~~said~~ isolating includes etching of at least a portion of ~~said~~ the at least one wafer-level redistribution circuit and ~~said~~ the outer passivation layer.

21. (Currently Amended) A method for isolating nonfunctional dice from a wafer-level testing configuration, comprising:

forming at least one wafer-level redistribution circuit on each of ~~said~~ a plurality of dice for interconnection with others of ~~said~~ the plurality of dice, ~~said~~ the at least one wafer-level redistribution circuit including a redistribution circuit for coupling at least one die contact to a respective bumped contact, a bus conductor traversing each of ~~said~~ the plurality of dice for electrically coupling with at least another one of ~~said~~ the plurality of dice and at least one other bus conductor for coupling ~~said~~ the redistribution circuit to ~~said~~ the bus conductor; and

isolating ~~at~~ the at least one die contact on each nonfunctional die of ~~said~~ the plurality of dice.

22. (Currently Amended) The method, as recited in claim 21, further comprising forming an outer passivation layer over ~~said~~ the at least one redistribution circuit and ~~said~~ the at least one other bus conductor.

23. (Currently Amended) The method, as recited in claim 22, wherein ~~said~~ the outer passivation layer is selectively removable over at least a portion of one of ~~said~~ the at least one redistribution circuit and at least one other bus conductor for forming an electrical open circuit between ~~said~~ the at least one die contact and ~~said~~ the at least one other bus conductor when a die of ~~said~~ the plurality of dice is determined to be defective.

24. (Currently Amended) The method, as recited in claim 23, wherein ~~said~~ isolating includes etching ~~said~~ the at least one redistribution circuit to form ~~said~~ the electrical open circuit.

25. (Currently Amended) The method, as recited in claim 23, wherein ~~said~~ isolating includes ablating ~~said~~ the at least one redistribution circuit by a laser to form ~~said~~ the electrical open circuit.